WHAT IS CLAIMED IS:

1. A method of forming a semiconductor device, the method comprising:

providing a substrate;

forming a SiGe surface layer on the substrate;

depositing a high-k dielectric layer onto the SiGe surface layer;

forming an oxide layer between the high-k dielectric layer and an unreacted portion of the SiGe surface layer, the oxide layer being formed during one or both of said depositing and an annealing process after said depositing; and

forming an electrode layer on the high-k dielectric layer.

2. The method according to claim 1, wherein the substrate is provided with an initial oxide layer prior to forming the SiGe surface layer.

3. The method according to claim 1, wherein forming the SiGe surface layer comprises performing thermal chemical vapor deposition, plasma-enhanced chemical vapor deposition, atomic layer deposition, or sputtering.

4. The method according to claim 1, wherein forming the SiGe surface layer comprises exposing the substrate to a process gas including a Ge-containing gas.

5. The method according to claim 4, wherein the Ge-containing gas comprises at least one of GeH_4 or $GeCl_4$.

6. The method according to claim 4, further comprising annealing the substrate either during said exposing, after said exposing, or both during and after said exposing.

7. The method according to claim 4, wherein the process gas further comprises a Si-containing gas.

8. The method according to claim 7, wherein the Si-containing gas comprises at least one of SiH_4, Si_2H_6, or SiH_2Cl_2.

9. The method according to claim 1, wherein the Ge content in the SiGe surface layer is less than about 10at.%.

10. The method according to claim 1, wherein the SiGe surface layer comprises a plurality of SiGe sublayers each with different Ge content.

11. The method according to claim 1, wherein the SiGe surface layer comprises a graded Ge content.

12. The method according to claim 11, wherein the SiGe surface layer has an average Ge content less than about 10at.%.

13. The method according to claim 1, wherein the SiGe surface layer is less than about 1000 angstroms thick.

14. The method according to claim 1, wherein the SiGe surface layer is between about 10 angstroms and about 300 angstroms thick.

15. The method according to claim 1, wherein the high-k dielectric layer comprises at least one of HfO_2, $HfSiO_x$, ZrO_2, $ZrSiO_x$, TiO_2, Ta_2O_5, Al_2O_3, or SiN.

16. The method according to claim 1, wherein the high-k dielectric layer is between about 5 angstroms and about 60 angstroms thick.

17. The method according to claim 1, wherein the providing comprises introducing a Si substrate into a process chamber of one of a single wafer processing system and a process chamber of a batch-type processing system.

18. The method according to claim 1, further comprising etching the electrode layer and the high-k dielectric layer.

19. The method according to claim 1, wherein the oxide layer is formed during the annealing process by exposing the substrate to an oxygen-containing gas.

20. A method of forming a semiconductor device, the method comprising:

providing a substrate;

forming a SiGe surface layer on the substrate;

depositing a high-k dielectric layer onto the SiGe surface layer;

annealing the substrate having the SiGe surface layer and high-k dielectric thereon; and

forming an electrode layer on the high-k dielectric layer,

wherein at least one of the depositing and the annealing comprises exposing the substrate to an oxygen-containing gas to form an oxide layer between the high-k dielectric layer and an unreacted portion of the SiGe surface layer.

21. A semiconductor device comprising:

a substrate having a SiGe surface layer with an unreacted portion;

a high-k dielectric layer on the SiGe surface layer;

an oxide layer between the high-k dielectric layer and the unreacted portion of the SiGe surface layer; and

an electrode layer on the high-k dielectric layer.

22. The semiconductor device according to claim 21, wherein the Ge content of the SiGe surface layer is less than about 10at.%.

23. A processing tool for forming a semiconductor device, comprising:

at least one processing system configured to form a SiGe surface layer on a substrate, to deposit a high-k dielectric layer onto the SiGe surface layer, to form an electrode layer on the high-k dielectric layer, to anneal the substrate, and to form an oxide layer between the high-k dielectric layer and

an unreacted portion of the SiGe surface layer either during said deposit, during said anneal, or during both said deposit and anneal;

a transfer system configured for transferring the substrate; and

a controller configured to control the processing tool.

24. The processing tool according to claim 23, wherein the at least one processing system comprises at least one of a single wafer processing system or a batch type processing system.

25. A processing tool for forming a semiconductor device, comprising:

means for forming a SiGe surface layer on a substrate;

means for depositing a high-k dielectric layer onto the SiGe surface layer;

means for performing an annealing process,

means for transferring the substrate; and

means for controlling the processing tool so that an oxide layer is formed between the high-k dielectric layer and an unreacted portion of the SiGe surface layer either during said depositing , during said performing, or during both said depositing and performing.